Decreasing of Frequency Variation in High-Speed Ring Oscillator using Bandgap Reference

Melikyan V.1, Balabanyan A.1, Babayan E.1, Durgaryan A.2
1Department of Microelectronics, State Engineering University of Armenia, Yerevan, Armenia, e-mail: vazgenm@synopsys.com, abrahamb@synopsys.com, edbab@synopsys.com
2Department of Radiophysics, Yerevan State University, Yerevan, Armenia, e-mail: armend@synopsys.com

Abstract – Techniques for decreasing of high-speed ring oscillator frequency variation are presented. Power supply is responsible for most of external noise and circuit parameters variation; hence its compensation can substantially stabilize the circuit. In the first case the oscillator is simulated with power supply of standard +/-10% voltage variation. In second case a bandgap reference is used for the oscillator power supply. Both scenarios are simulated, the results compared and discussed.

Keywords – PVT compensation; bandgap reference; voltage controlled oscillator

I. INTRODUCTION

With continuous shrinking of CMOS technology sizes and increasing operating frequencies of integrated circuits effect of noise and process, voltage, temperature (PVT) [1,2] variations on circuit parameters become more perceptible. One of the most important characteristics of high-speed integrated circuits is stable frequency.

As a typical high-speed circuit a voltage controlled oscillator (VCO) [1] was chosen. By power supply compensation VCO frequency became much more resilient to PVT variations. The main compensated parameter is power supply voltage which exhibits less than +/-3,2% variation over 110 process corners.

II. PVT VARIATION EFFECTS

In order to assess effect of PVT variations in high speed systems a classical voltage controlled oscillator (VCO) has been selected. This choice is justified by the fact that timing parameters of a CMOS VCO are known to be very prone to PVT changes. Besides, the VCO’s are widely used in modern integrated phase locked loops (PLL), where stable AC parameters are pivotal. The considered VCO topology, Fig. 1, is a classical 5-stage differential ring oscillator based solution. For the VCO output frequency the following expression takes place:

$$F_{VCO} \sim \frac{l_{tail}}{2 \cdot C_n \cdot N \cdot V_{swg}}$$

(1)

where $$F_{VCO}$$ is the output frequency, $$l_{tail}$$ is the tail current source current; $$C_n$$ is the total capacitance at the VCO delay stage output, $$N$$ is the number of stages and $$V_{swg}$$ voltage swing in the VCO output. For saturated current tails:

$$I_{tail} \sim k(V_{gs} - V_{th})^2 \cdot (1 + \lambda \cdot V_{gs}),$$

(2)

$$V_{gs} = V_{dd} - V_{bp} = f(V)$$

$$V_{th} = f(P,T)$$

(3)

$$C_{ox} = f(P)$$

where $$V_{gs}$$ is the gate-source voltage, $$V_{ds}$$ is the drain-source voltage, $$V_{th}$$ is the threshold voltage, $$V_{bp}$$ is the bias voltage for PMOS transistor, $$\lambda$$ is the modulation coefficient, $$V_{dd}$$ is the power supply voltage, $$C_{ox}$$ is the gate oxide capacitance, $$P$$ is the process, $$T$$ is the temperature. $$V_{gs}$$ is a function of supply voltage, $$V_{th}$$ is a function of process and temperature, $$C_{ox}$$ is a function of process (depending on gate thickness variations). Hence full compensation is possible only if all process, voltage and temperature, variations are canceled. Here canceling the voltage variation and its effect on VCO is presented. Quantitative assessment is presented.

III. SUGGESTED SOLUTION

The schematic solution considered in this paper consists of three fundamental blocks: bandgap reference generator (BGR), drive strength buffer and the VCO itself.

For the BGR a classical operational amplifier based solution has been adopted. For the drive strength buffer, a two stage amplifier is used, Fig. 2. The amplifier is used as a voltage replicating circuit. Due to feedback connection its output voltage susceptibility to PVT fluctuations are practically the same as that of the BGR output, ~1.29V. The drive strength buffer is responsible for feeding the main current consuming circuitry, (in this case VCO).

More advanced solution is presented in Fig. 3. It uses an operational amplifier in feedback to generate bias current through the resistor $$R_{ref}$$, which is equal to $$V_{ref} / R_{ref}$$ since the amplifier forces voltage equal to $$V_{ref}$$ at the resistor. The bias currents are fed to the ring oscil-
lator delay cells. This results in VCO frequency being dependent on the $R_{ref}$ value. On chip resistors are less subject to process and temperature changes compared to the MOS devices hence it is possible to achieve improved PVT compensation. In systems like DDR [3] external resistors are also available. Using external resistors will allow for substantial compensation of current and hence VCO frequency [4].

![Figure 2. Compensated VCO circuit](image)

The VCO supply voltages as well as $V_{bn}$ and $V_{bp}$ control voltages are governed by BGR generated reference, thus they are practically free of supply voltage variations.

![Figure 3. Operational amplifier for VCO current compensation](image)

### IV. SIMULATION RESULTS

Simulations have been performed using circuit level simulator Hspice [5] for 110 PVT corners, including SS (slow-slow), TT (typical-typical), FF (fast-fast), SF (slow-fast), FS (fast-slow) with supply voltage and temperature variations. Fig. 4 shows comparison of output frequency vs. simulation corner plots, for both PVT compensated and non-compensated circuits. The main PVT corners are encircled. It can be clearly seen that the compensated circuit has frequency stability noticeably superior to the uncompensated one. Numerical results are presented in the table I. The total variation for the PVT compensated circuit is 5,75GHz whereas the same result for the initial circuit is 9,14GHz. The improvement is more than 37%.

Table I shows single delay cell average current values for the main PVT corners. As it can be seen the maximal current for the proposed solution is decreased by about 47uA (~235uA for 5-stage VCO) which makes about 22%. Considering supply voltage compensation inherent to the BGR systems the maximal power consumption is decreased by ~28,7% (taking into account 10% supply voltage drift in non compensated circuits).

![Figure 4. Comparison of output frequency for PVT compensated and non-compensated circuits](image)

<table>
<thead>
<tr>
<th>Corner</th>
<th>SS</th>
<th>TT</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Freq (non-compensated) GHz</td>
<td>6,87</td>
<td>11,01</td>
<td>16,01</td>
</tr>
<tr>
<td>Freq (compensated) GHz</td>
<td>8,32</td>
<td>11,11</td>
<td>14,07</td>
</tr>
<tr>
<td>$I_{vco}$ (non-compensated) uA</td>
<td>76</td>
<td>134</td>
<td>216</td>
</tr>
<tr>
<td>$I_{vco}$ (compensated) uA</td>
<td>101</td>
<td>133</td>
<td>169</td>
</tr>
</tbody>
</table>

Output frequency values of compensated and non-compensated VCOs and single delay cell average current values for the main PVT corners

### V. CONCLUSIONS

Effects of PVT variations on frequency stability of high speed voltage controlled oscillators have been studied. A simple, bandgap reference based solution for PVT variation effect cancelation has been studied and its efficiency has been assessed. Simulations over multiple PVT corners have shown frequency variation decreased by over 37% and maximal power consumption decrease by more than 28%.

### REFERENCES